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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/824,012	04/14/2004	Dolly Wu	AD-320J	5947

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EXAMINER	
WELLS, KENNETH B	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 11/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H:A

Office Action Summary	Application No.	Applicant(s)	
	10/824,012	WU ET AL.	
	Examiner	Art Unit	
	Kenneth B. Wells	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 April 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/14/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-23 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, it is misdescriptive, and thus indefinite, to recite that the integrating switched capacitor circuit is connected to the summing junction, i.e., as shown instant figure 5, the integrating switched capacitor circuit includes the summing junction. Also in claim 1, "said input of said cascoded amplifier circuit" lacks antecedent basis.

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the third switch of claim 7 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure

number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 14 and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by He.

Note figure 3, where the cascoded amplifier circuit is circuit AMP1 (note figure 1 of this reference which shows the cascoded amplifier circuit); the summing junction is at node 70; the correlated double sampling capacitor circuit is formed by the combination of switches SW2, SW3, SW10, SW5 and SW6, and capacitors C2 and C3; and the integrating switched capacitor circuit is formed by the combination of switches SW11, SW1 and capacitor C1. The recited offset capacitor is capacitor C2.

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-5, 13, 14, 16 and 18-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over any one of Myers et al, McCartney and Early et al in view of He.

In Myers et al, note Fig. 4, where the recited amplifier is A2; the recited summing junction is the node between switches S1 and S4; the recited correlated double sampling capacitor circuit is formed by the combination of

switches S4, S5, S9, S6, S7, S8 and capacitors C2 through C4; and the recited integrating switched capacitor circuit is formed by the combination of switches S1 through S3 and S10 through S13 and capacitors C1, C5 and C6 (and also amplifiers A1 and A3). The recited offset capacitor is C2.

In McCartney, note Fig. 5, where the recited amplifier is amplifier 12; the recited summing junction is node N3; the recited correlated double sampling capacitor circuit is formed by the combination of switches 511, 512 and capacitor C3; and the recited integrating switched capacitor circuit is formed by the combination of switch 513 and capacitor C2. The recited offset capacitor is capacitor C3.

In Early et al, note Fig. 1, where the recited amplifier is amplifier 12; the recited summing junction is the node between switch 13 and capacitor 14; the recited correlated double sampling capacitor circuit is formed by the combination of switches 15, 16, 22, 24, 26, 27 and capacitors 14, 17 and 23; and the recited integrating switched capacitor circuit is formed by the combination of switches 30, 31 and 33 and capacitors 29 and 32. The recited offset capacitor is capacitor 14.

Not disclosed by each of these references is that

the amplifier is a cascoded amplifier. Such would have been obvious, however, in view of He who teaches such a well-known circuit. The motivation for using a cascoded amplifier is to obtain the advantages associated with such a circuit, i.e., lowered capacitance and improved frequency response, as compared to a differential amplifier circuit without cascode transistors.

As to claims 2-5, the limitations of these claims do not define patentably over the above-noted references because they merely recite well-known details of a variable capacitor circuit (obvious motivation to make the capacitors variable, i.e., to provide felxibility of the various capacitance values).

As to claims 16 and 18-23, these claims also do not define patentably over the above-noted references because they are all well-known features of cascoded amplifier circuits (of which fact official notice is taken).

5. Claims 1-6, 13, 14, 16 and 18-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagaraj or "Electronics Letters" (cited by applicant) in view of He.

In Nagaraj, note Fig. 7, where the recited amplifier is the unnumbered amplifier with its output connected to V0

(through a switch controlled by signal phi 1); the recited summing junction is the node between the two switches at the bottom middle of the figure; the recited correlated double sampling capacitor circuit is formed by the combination of the switches connected between the input and output of the above-noted amplifier which are controlled by signals phi 1 and phi 2 and the capacitor directly connected to the amplifier output; and the recited integrating switched capacitor circuit is formed by the combination of all of the remaining circuitry in Fig. 7. The recited offset capacitor is the capacitor at the bottom middle of Fig. 7 connected directly to the inverting input of the amplifier. The hold capacitor is the capacitor having one of its plates directly connected to the output of the amplifier.

In "Electronic Letters", note Fig. 1, where the recited amplifier is amplifier A1; the recited summing junction is the node between capacitors C2 and C3; the recited correlated double sampling capacitor circuit is formed by the combination of the two switches directly connected to one plate of the capacitor C4 (which are controlled by signals phi 1 and phi 2) and the capacitors C3 and C4; and the recited integrating switched capacitor

circuit is formed by the switches to the left of capacitor C3 in combination with capacitor C2. The recited offset capacitor is capacitor C3. The hold capacitor is capacitor C4.

Not disclosed by these references is that the amplifier is a cascoded amplifier. Such would have been obvious, however, in view of He who teaches such a well-known circuit. The motivation for using a cascoded amplifier is to obtain the advantages associated with such a circuit, i.e., lowered capacitance and improved frequency response, as compared to a differential amplifier circuit without cascode transistors.

As to claims 2-5, the limitations of these claims do not define patentably over Nagaraj because they merely recite well-known details of a variable capacitor circuit (obvious motivation to make the capacitors variable, i.e., to provide felxibility of the various capacitance values).

As to claims 16 and 18-23, these claims also do not define patentably over Nagaraj because they are all well-known features of cascoded amplifier circuits (of which fact official notice is taken).

6. Claims 1-5, 9, 13, 14, 16 and 18-23 are rejected under

35 U.S.C. 103(a) as being unpatentable over Pernigotti et al in view of He.

In Pernigotti, note Fig. 5, where the recited amplifier is the unnumbered amplifier with its non-inverting input terminal connected directly to Vref; the recited summing junction is the node between Vin and capacitor C1; the recited correlated double sampling capacitor circuit is formed by the combination of the switch controlled by signal phi 5, the switch controlled by signal phi 4 connected between capacitor C1 and Vref, and the capacitor C1; and the recited integrating switched capacitor circuit is formed by the combination of the switches controlled by signals phi 1, phi 2a and phi 2b, the capacitors C2a, C2b, and the switch controlled by signal phi 4 connected between the summing junction and the inverting input terminal of the above-noted amplifier. The recited offset capacitor is the capacitor C1. Note also additional input Vref applied to the summing junction when the switch controlled by phi 3 is closed.

Not disclosed by Pernigotti et al is that the amplifier is a cascoded amplifier. Such would have been obvious, however, in view of He who teaches such a well-known circuit. The motivation for using a cascoded

amplifier is to obtain the advantages associated with such a circuit, i.e., lowered capacitance and improved frequency response, as compared to a differential amplifier circuit without cascode transistors.

As to claims 2-5, the limitations of these claims do not define patentably over Pernigotti because they merely recite well-known details of a variable capacitor circuit (obvious motivation to make the capacitors variable, i.e., to provide felxibility of the various capacitance values).

As to claims 16 and 18-23, these claims also do not define patentably over Pernigotti because they are all well-known features of cascoded amplifier circuits (of which fact official notice is taken).

7. Claims 7, 8, 10-12 and 17 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenneth B. Wells whose telephone number is (571)272-1757. The examiner can normally be reached on Monday through Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan, can be reached at (571)272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kenneth B. Wells
Primary Examiner
Art Unit 2816

November 12, 2005